UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,872	09/30/2003	Jimmie Earl DeWitt JR.	AUS920030487US1	6779

35525 7590 07/13/2007

IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2191	

MAIL DATE	DELIVERY MODE
07/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,872	DEWITT ET AL.	
	Examiner	Art Unit	
	Ted T. Vo	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 11/10/06, 12/15/06, 1/25/07, 3/27/07
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is reopened and it is addressed to Claims filed on 09/05/06, in response to the Appeal brief filed on 03/05/2007.

Claims 1-25 are pending in the application.

Response to Arguments

2. The Brief, as part of the Application record, shows that Applicants contented that the medium included a transmission-type media such digital and analog communication links, wireless communications links, radio frequency, light wave transmissions, etc are statutory.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. The claims 24-25 are rejected under 35 U.S.C 101 because the claimed invention is directed to non-statutory subject matter.

As per claims 24-25: Claims recite a produce that in carried in a medium included a transmission-type media such digital and analog communication links, wireless communications links, radio frequency, light wave transmissions, etc. The claims fail to meet claimed statutory under 35 U.S.C. 101.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 4, 11, 18 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Specific critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Claims 4, 11, and 18 recite a second range, and it appears the second range is not the same with the range that is determined in the first time. According to appeal, Applicants show that the specification does not teach second range. These claims that recite the second range fail to be enablement because second range is not included in the disclosure.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4, 11, 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4, 11, and 18,are indefinite because the claims recite the limitation "second range" that lacks antecedent basis in the specification. To expedite the examination, the interpretation for this limitation is, "within the same contiguous range of instructions".

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Intel, "Intel IA-64 Architecture Software Developer's Manual", Revision 1.1, July 2000, IDS submitted by Applicants.

CLAIM 1: Intel discloses profiling, which has performance counters (p.6-3, sec. 6.1.1.3) used to count occurrence of some events within a specific instruction address range ('*contiguous range of instructions*' (See p. 6-5, sec. 6.1.2: Profiling)). Processor has a program counter that increments every execution (conventional). Intel discloses a method in a data processing system for monitoring execution of instructions. An instruction for execution is identified (See Figure 6-4, p. 6-9, Current Instruction AND Event). It is determined whether the instruction is within a contiguous range of instructions (See Figure 6-4, p. 6-9, Current Instruction AND Event AND Instruction Address: → Check: YES, all of above are true: This explained that when a current instruction is entered for execution, it is checked if it is within a specific addressed range and is an event), and execution information relating to the instruction is generated if the instruction is within the contiguous range of instructions (See Figure 6-4, checked if event monitor is enabled – See Sec. 6.1.3: Event Qualification: See last bullet: It means that the performance counter counts the event, except situations such as overflow interrupt, pollute, etc.

As per Claim 2: Intel discloses, *the generating step comprises: counting each event associated with execution of the instruction if the instruction is within the contiguous range of instructions* (See p. 6-8, second bullet).

As per Claim 3: Intel discloses, *The method of claim 2, wherein the counting step comprises: sending a signal from an instruction cache to a performance monitor unit* (See p. 6-22, a PMC used to monitor instruction cache L1, where this PMC is used in the condition for counting the events in the Figure 6-4 and Figure 6-5)*; and the performance counter unit tracking the counting of each event associated with an execution of the instruction if the instruction is within the contiguous range of instructions* (See result YES, and counter PMD).

As per Claim 4: Intel discloses, *The method of claim 1 further comprising: determining whether the instruction is within a second contiguous range of instructions* (See Figure 6-4, and Figure 6-5, "Address range check". This address range check provide the event/instructions within the range is counted); *and generating the execution information relating to the instruction if the instruction is within the second contiguous range of instructions* (i.e. the instruction in the ranged in count, out of the range is not counted according to the figures 6-4 and 6-5).

As per Claim 5: Intel discloses, *The method of claim 1, wherein the execution information includes at least one of a number of visits to the range of instructions and a number of times the instruction has been executed* (Clearly, whenever the same instruction is passed, the counter is incremented).

As per Claim 6: Intel discloses, *The method of claim 1, wherein the determining step comprises: comparing an address of the instruction to set of addresses in a set of registers in a processor to determine whether the instruction is in the contiguous range of instructions.*, see p. 6-11, sec. 6.1.3.2.

As per Claim 7: Intel discloses, *The method of claim 6 further comprising: setting the set of registers using a performance tool.*, Setting via data breakpoint registers

CLAIM 8: Intel discloses a method in a data processing system for monitoring access to data in memory location An access to data in a memory location is identified (See p. 6-9, Figure 6-4: Data addresses. See p. 6-10, Figure 6-5, "Memory Event"). It is determined whether the memory location is within a contiguous range of memory locations (Figure 6-4: Data addresses. Figure 6-5, "Data Address Range Check"), and information relating to the memory location is generated if the memory location is within the contiguous range of memory locations (See in the Figure 6-5, Counter PMD).

As per Claims 9-14: Intel discloses Claims 9-14. See rationale addressed in Claims 2-7 above.

CLAIM 15: it broadly recites "means"; however, it is in the same manner of the claim 1.

See rationale addressed in the rejection of Claim 1.

As per Claims 16-21: Intel discloses Claims 16-21. See rationale addressed in Claims 2-7 above.

CLAIM 22: Intel discloses The subject matter of claim 22 is directed to a data processing system for monitoring access to data in memory locations. The data processing system includes identifying means for identifying an access to data in a memory location (See p. 6-1, "processor data and Instruction caches"), and determining means for determining whether the memory location is within a contiguous range of memory locations (See Figure 6-5: "Memory event" AND "Address Range Check"). A generating means generates information relating to the memory location if the memory location is within the contiguous range of memory locations (See in the Figure 6-5, Counter PMD).

As per Claim 23: Intel discloses Claim 23. See rationale addressed in Claim 2 above.

CLAIM 24: it recites "a computer program product"; however, it is in the same manner of the claim 1. See rationale addressed in the rejection of Claim 1.

CLAIM 25: it recites "a computer program product"; however, it is in the same manner of the claim 8. See rationale addressed in the rejection of Claim 8.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708.

The facsimile number for the organization where this application or proceeding is assigned is the Central Facsimile number **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TTV
July 06, 2007

TED VO
PRIMARY EXAMINER